A Three Levels Diode Clamped Inverter For Renewable Energy System

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Abstract— This paper describes a diode-clamped three-level inverter-based a direct integration scheme for renewable energy systems. And a closed loop control of space vector pulse width modulation (SVPWM) based diode clamped three level inverter for AC module applications. The space vector diagram of three-level inverter is simplified into two-level inverter. So the selection of switching sequences is done as conventional two-level SVPWM method. Thus, the proposed algorithm reduces the complexity involved in the PWM algorithm. Two level switching loss minimized PWM (SVPWM) method is extended to the three level inverter. The neutral point voltage unbalance problem which are the inherent of three level inverter are solved successfully in this method by some special means. The simulation and experimental results show the proposed method is feasible and suitable for high power three level. The operation and performance of the proposed converter has been verified by experimental and simulation results. The simulation results show its capability in voltage generation and voltage swell/sag compensation

Keywords— Boost converter, neutral point clamped inverter, space vector modulation (SVM), renewable source

INTRODUCTION

MANY industrial applications are require higher power converters(inverters) which are now almost exclusively implemented using one of the multilevel types. Multilevel converters offer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters and operation at higher dc voltages using series connection of a basic switching cell of one type or another [1]–[4].

Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter [5],[6], the diode clamped inverter [7] and the capacitor clamped inverter [8]. Among the three, the three level diode clamped [also known as the neutral point clamped (NPC)] inverter has become an established topology in medium voltage drives and is arguably the most popular [16]certainly for three-level circuits.

However, the NPC inverter is constrained by its inability to produce an output line-to-line voltage greater than the dc source voltage. For applications where the dc source is not always constant, such as a fuel cell [20], [21], photovoltaic array [22], and during voltage sags, etc., a dc/dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favorably located [23], [24]. This increases the system complexity and is desirable to eliminate if possible.

The space vector modulation (SVM) technique uses a fixed frequency in synthesizing the reference vector, enabling many power applications to lower their switching losses. This clearly improves the efficiency, which is vital for high power applications such as DC/AC converters that are interconnected to power systems through transformers. While the SVM can be practically considered as a voltage based technique for the AC/DC converter output, one should obtain the reference voltage vector based on the required objectives of a certain application. Unlike the voltage-based SVM techniques, the current-based modulation techniques (e.g hysteresis modulation) impose high losses despite their easy approach towards providing required reference current vector. Hence, the problem can be narrowed down to two problems for the SVM technique; first, provision of a three-phase reference voltage vector for the AC/DC converter output, and, second, making up the provided reference vector using the different switching status produced by a three-dimensional SVM technique. The instantaneous phase quantities *abc* are transferred to the so called αβo space to achieve a better distinction of zero sequence component for four-wire systems, in particular the active power filter. Sinusoidal PWM has been a very popular technique used in AC motor control. This relatively unsophisticated method employs a triangular carrier wave modulated by a sine wave and the points of intersection determine the switching points of the power devices in the inverter. However, this method is unable to make full use of the inverter's supply voltage and the asymmetrical nature of the PWM switching characteristics produces relatively high harmonic distortion in the supply. Three-phase systems are well known by their use in electric power generation transmission and distribution. Applications including distributed generation and uninterruptable power supplies etc

II. DIODE CLAMPED INVERTER

A three level diode clamped inverter circuit diagram is shown in Fig.1. Each leg is composed of two upper and lower switches with anti-parallel diodes. Two series dc link capacitors split the dc bus voltage in half and six clamping diodes confine the voltages across the switch within the voltages of the capacitors.

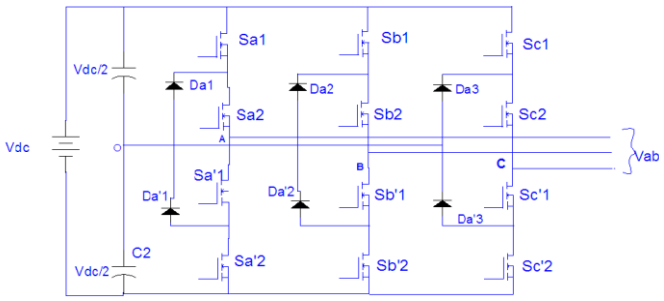

Fig 1: Three level DCM inverter

The necessary conditions for the switching states are that the dc link capacitors should not be shorted and the output current should be continuous

A.Review of svpwm algorithm concept

SVPWM refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and or currents applied to the phases of an AC motor and to provide more efficient use of supply voltage. There are two possible vectors called zero vector and Active 58 vector. The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching patterns One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of Vref in the same period. Therefore, space vector PWM can be implemented by the following steps:

Step 1. Determine V_d, V_q, V_{ref}, and angle (α)

At sector I, V1 and V2 are voltage vectors. Assume Vref makes phase angle difference with V1. This Vref can be calculated using vector d Axis q Axis B C A Vref calculus by referring Figure 4.7. „Tz„is switching time interval at which output voltage of inverter is constant. T1 and T2 are switching time duration of voltage space vectors V1 and V2.

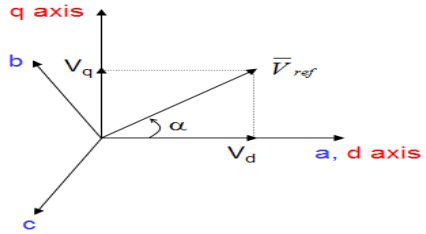

Fig 2 :Dq and ABC Reference Frame

The reference voltage space vector or sample, which is as shown in Fig.2 represents the corresponding to the desired value of the fundamental components for the output phase voltages. In the space vector approach this can be constructed in an average sense. *Vref* is sampled at equal intervals of time,*Ts* referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different time durations with in a sampling time period such that the average vector produced over the sampling time period is equal to the sampled value of the *Vref* , both in terms of magnitude and angle. It has been established that the vectors to be used to generate any sample are the zero voltage vectors and the two active voltage vectors forming the boundary of the sector in which the sample lies. As all six sectors are symmetrical, the discussion is limited to the first sector only. For the required reference voltage vector, the active and zero voltage vectors times can be calculated as in

$$V_d=Van-V_{bn}.COS60.V_{cn}.COS60 \quad (1)$$

$$V_d = V_{an}-\frac{1}{2}V_{bn}-\frac{1}{2}V_{cn} \quad (2)$$

$$V_q = 0_+ V_{bn}.COS60.V_{cn}.COS60 \quad (3)$$

$$V_q = V_{an}-\frac{\sqrt{3}}{2}V_{bn}-\frac{\sqrt{3}}{2}V_{cn} \quad (4)$$

The zero vectors are not present in all the sectors, where these are present in three level inverters. In order to simplify the above equations, the space vector plane of three level inverter shown in Fig.3 is subdivided into six sectors each of 60 degree as shown in Fig.5 each sector S, S= 1,2…,6 are consists of one pivot vector *Vs* and other six vectors of sector 1 is reproduced in Fig.5 (a). The vectors of the other sectors are phase displayed by $\pi/3$ radians.

Step 2. Determine time duration T_1, T_2, T_0

In space vector PWM technique, the required space vector is synthesized by two adjacent vectors and null vector. Switching time duration at Sector 1 From Figure 3, the switching time duration can be calculated as follows:

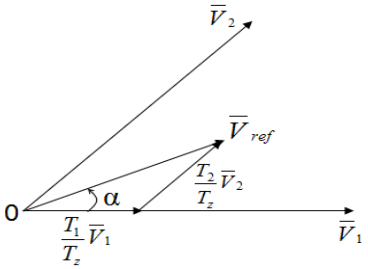

Fig 3: Reference Vector with Respect to voltage

According to volt-sec balance principle,

$$\int_0^{Tz}\overline{V}ref\,dt = \int_0^{T1}\overline{V}1dt + \int_{T1}^{T1+T2}\overline{V}_2dt+\int_{T1+T2}^{Tz}\overline{V}_0dt \quad (6)$$

$$\therefore T_Z.V_{ref} = (T_1.\overline{V}_1+T_2.\overline{V}_2) \quad (7)$$

$$T_Z.\left|V_{ref}\right|.\begin{bmatrix}cos(\alpha)\\ sin(\alpha)\end{bmatrix}=T_1.\bar{V}_1\begin{bmatrix}1\\0\end{bmatrix}+T_2.\bar{V}_2\begin{bmatrix}\cos\left(\frac{\pi}{3}\right)\\ \sin\left(\frac{\pi}{3}\right)\end{bmatrix} \quad (8)$$

$$\therefore T_1=T_Z.\frac{\left|\overline{V}ref\right|}{\bar{V}dc}.\frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \quad (9)$$

$$\therefore T_2=T_Z.\frac{\left|\overline{V}ref\right|}{\bar{V}dc}.\frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \quad \text{where} 0\leq \alpha \leq 60°, T_z=\frac{Ts}{2}\&\frac{1}{fs} \quad (10)$$

$$\therefore T_0=T_z-(T_1+T_2) \quad (11)$$

Where,

T1 is the time for which V 1 is applied

T2 is the time for which V 2 is applied

T0 is the time for which null vector is applied

Ts is the sampling time

Similarly switching time duration at any sector can be calculated

Step 3. Determine the switching time (S_1 to S_6) sectors

By selecting the space vectors and their times calculated, switching sequence is going to be the next step to arrange. A typical seven-segment switching sequence and inverter output voltage waveforms for Vref in sector I is shown in Figure 3 where V1 and V2 synthesize Vref. The sampling period TS for selected vectors can be divided into the seven segments. Note that the null time has been conveniently distributed between the V0 and V7 vectors to describe the symmetrical pulse width (to produce minimal output harmonics.)

Table 3.3 Switching Time Calculation at each Sector

sector	Upper switches (S_1,S_2,S_3)	Lower Switches (S_4,S_6,S_2)
1	$S_1= T_1 + T_2 + T_0/2$ $S_3= T_2 + T_0/2$ $S_5= T_0/2$	$S_4=T_0/2$ $S_6=T_1+T_0/2$ $S_2= T_1+T_2 + T_0/2$
2	$S_1= T_1 + T_0/2$ $S_3= T_1 +T_2 + T_0/2$ $S_5= T_0/2$	$S_4= T_1+T_0/2$ $S_6= T_0/2$ $S_2= T_1+T_2 + T_0/2$
3	$S_1= T_0/2$ $S_3= T_1 + T_2 + T_0/2$ $S_5= T_2 + T_0/2$	$S_4= T_1+T_2 + T_0/2$ $S_6= T_0/2$ $S_2= T_1+T_0/2$
5	$S_1= T_1 + T_0/2$ $S_3= T_0/2$ $S_5= T_1 +T_2 + T_0/2$	$S_4= T_1+T_0/2$ $S_6= T_1+T_2 + T_0/2$ $S_2= T_0/2$
6	$S_1= T_1 +T_2 + T_0/2$ $S_3= T_0/2$ $S_5= T_1 + T_0/2$	$S_4= T_0/2$ $S_6= T_1+T_2 + T_0/2$ $S_2= T_1+T_0/2$

B. Turning of PI Controller

The most widely used controller is still of PI controller type. Finding design methods which lead to the optimal operation of PI controllers is therefore of significant interest. For controller tuning simplicity, as well as optimality, is the important[14,15].To improve the system output response, cascade PI controller is used as shown in fig4.The simulation result will be analyzed clearly in last section

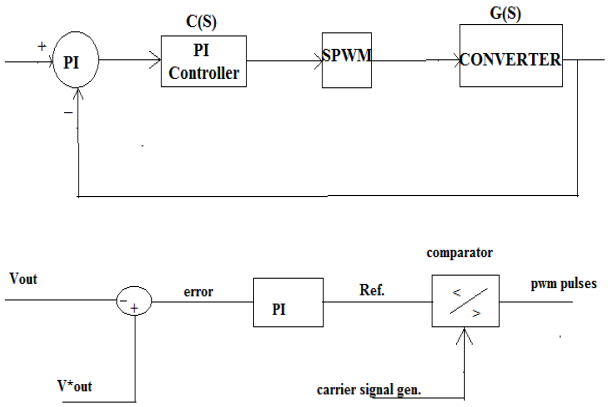

Fig 4 Block diagram of a PI Controller

III. VOLTAGE BALANCING PRINCIPLE

Fig. 4 shows the equivalent circuit of a three-phase *n*-level DCMC. The three-phase PWMsignals would generate a current conduction path between one input node of the voltage source inverter (VSI) and an expected output voltage level. As shown in Fig.4,the equivalent model indicates that the switch routes the input to one node of the dc-link capacitor according to the PWM index. Therefore, the operating currents will charge or discharge the capacitors, which will influence the dc-link voltage equalization.

A.Minimum energy property

Assuming that all dc-link capacitors of the *n*-level DCMC have the same capacitance and voltage, the mathematical conditions are

$$C_1= C_2= \cdots = C_n=C \quad (9)$$

$$V_{C1}= \cdots = V_{Cn-1}=\frac{Vdc}{(n-1)} \quad (10)$$

The total energy stored in the capacitors would reach the minimum value when their voltages are balanced [34]

$$E=\frac{1}{2}\sum_{i=1}^{n-1} C_i V_{ci}^2 \quad C_1= C_2= \cdots = C_n=C \quad =\frac{Vdc}{2(n-1)} \quad (11)$$

$$V_{C1}= \cdots = V_{Cn-1}=\frac{Vdc}{(n-1)} \quad (12)$$

Define a positive-definite cost function *J* to indicate the Energy drift from the minimum in (11)

$$J=\frac{1}{2}C\sum_{i=1}^{n-1}\Delta V^2_{Ci} \quad (13)$$

which is the voltage deviation of capacitor C_i. If a definite negative ΔJ could be guaranteed through the proper PWM outputs, the voltages would fluctuate toward the balanced values.

$$\Delta V_{Ci}=V_{Ci}-\frac{Vdc}{(n-1)} \quad (14)$$

That is

$$\frac{dJ}{dt}=C\sum_{i=1}^{n-1}\Delta V_{Ci}\frac{dVci}{dt}=C\sum_{i=1}^{n-1}\Delta V_{Ci}\,i_{Ci}\leq 0 \quad (15)$$

where i_{Ci} is the current charge into capacitor C_i. This condition is called the minimum energy property for a balanced *n*-level DCMC. It could be used as the basic principle for dc-capacitor voltage balancing and control [9]. Once the voltages are unbalanced, the PWM fitting the condition defined in (14) will reduce *J* to zero, which means that the voltages are tended to be balanced. The optimal PWM vector is the one which would minimize the result of (14) among all of the redundant vectors.

IV. BASIC FUNCTION OF BOOST CONVERTER

The DC/DC boost converter only needs four external components: Inductor, Electronic switch, Diode and output capacitor. The converter can therefore operate in the two different modes depending on its energy storage capacity and the relative length of the switching period.

Mode 1 begins when IGBT's is switched on at t = 0 and terminates at t = ton. The equivalent circuit for the model is shown in Fig. 1.The inductor current I L(t) greater than zero and ramp up linearly. The inductor voltage is Vi Mode 2 begins when IGBT's is switched off at t=ton and terminates at t = ts.The inductor current decrease until the IGBT's is turned on again during the next cycle. The voltage across the inductor in this period is Vin-Vout . In steady state time integral of the inductor voltage over one time period must be zero.

$$V_i * t_{on}+(V_i-V_0) * t_{off}=0 \quad (16)$$

Where,
Vi : The input voltage, V.
Vo : The average output voltage, V.
Ton : The switching on of the IGBT's, sec
Toff : The switching off of the IGBT's, sec
Dividing both sides by Ts and rearranging items yield

$$\frac{Vo}{Vi}=\frac{Ts}{toff}=\frac{1}{1-D} \quad (17)$$

Where,
Ts : The switching period, s.
D : The duty cycle.

V. SIMULATION RESULTS AND DISCUSSION

Figure5 shows the Matlab Simulink model of the three-phase three level diode clamped multilevel inverter with the RLC load. The only assumption in this model is that the there is an ideal dc-voltage source at the dc link. The model consists of three phase leg average models, a model of load, and the high power modulation strategy SVPWM Technique. There are two models that were used for the simulations: The first model used for the simulations of the inverter mode of operation and the second is the SVPWM technique.DCM Inverter was designed & simulated successfully using MATLAB (SIMULINK) &following results(Fig 7-9) were generated. Simulation parameters are given in Table 1.

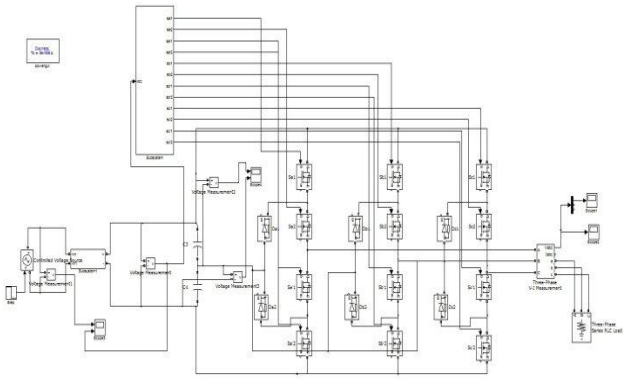

Fig 5: Simulink model of diode clamped inverter

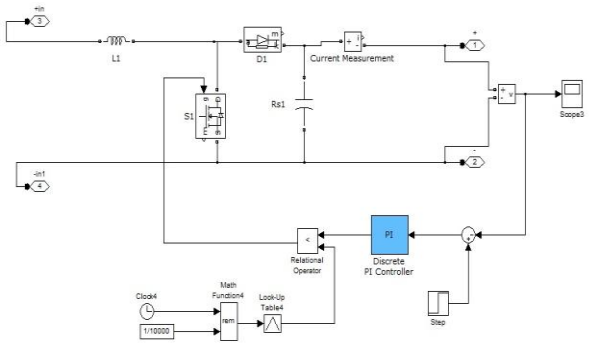

Fig 6: Simulink Model of Input Side Boost Converter

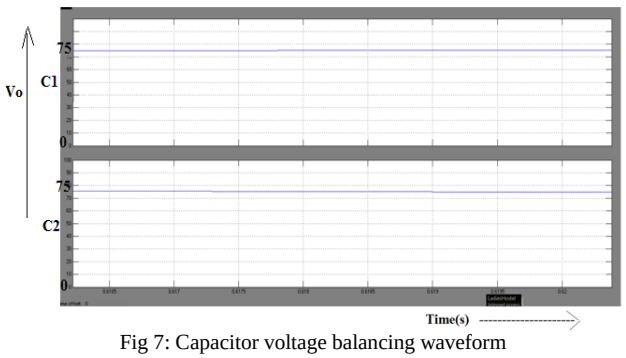

Fig 7: Capacitor voltage balancing waveform

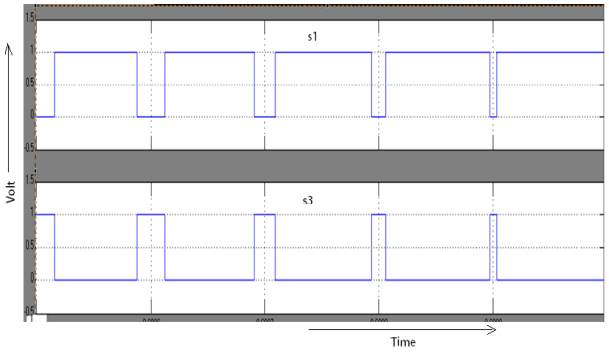

Fig 8: Inverter gate pulse s_1 and s_3

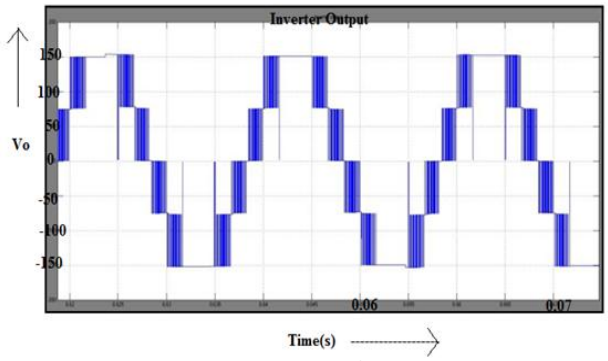

Fig 9: Inverter Output voltage waveform created with SVPWM

VI CONCLUSION

This thesis has demonstrated the state of the art of multilevel power converter technology. Mainly presented the theories behind multilevel converters, using the neutral point diode clamped converter as a basis. Advantages with the diode-clamped inverter are the high efficiency. The SVPWM algorithm in this frame is simple and more convenient in full digital fixed-point realization with low calculation cost The modulation chosen for the project, the space vector pulse width modulation, has good utilization of the DC link voltage, low current ripple and is relative easy to implement in the hardware. These features make it suitable for high-voltage high-power applications, such as renewable power generation.

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