Simulation of two multilevel topologies with selective harmonic reduction

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***Abstract*- Multilevel inverter is an inevitable part of power electronics, as it is widely used in many industrial applications. Multilevel inverter is more advisable when compared to the common inverter because of its reduced THD and hence multilevel inverter is always used to supply AC machines. Since the multilevel inverter is of that importance in industries, wide research had been doing for years to propose various topologies of multilevel inverter. These topologies were aiming at reducing number of switches, number of DC sources used and voltage across the switches which can ultimately reduce the THD. Out of various topologies that has been proposed by researchers, multilevel inverter in normal cascaded connection and multilevel inverter using series connected sub-multilevel topology with and without incorporating reduced harmonic reduction are taken up for comparison in this paper. These topologies are simulated in the paper and results are taken for comparison.**

I. INTRODUCTION

Multilevel inverter is an arrangement of power semiconductors and DC sources in a proper manner so as to get a stepped output voltage waveform in its output. Using of high level multilevel inverter is advisable as the level increases the distortion in voltage waveform decreases. Complexity of the control algorithm increases with increase in number of levels.[1], [3],[4],[6].

Various types of multilevel inverter is shown in the form of flowchart

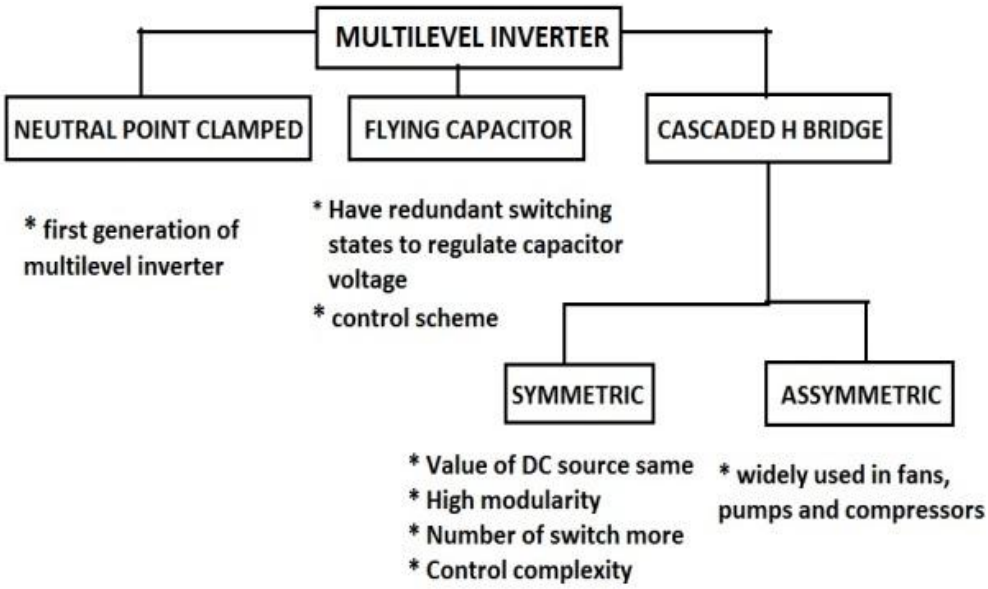


Figure 1. Flowchart showing basic topologies of multilevel inverter

Harmonic reduction method aims at eliminating selected harmonics and it also helps in reducing harmonics by switching the main switch once in a cycle. All the topologies that are simulated in this paper is at modulation index=1 and are of seven level.

II. SELECTIVE HARMONIC REDUCTION

Positive half cycle of seven level stepped output voltage waveform of a multilevel inverter is as shown in the figure 2

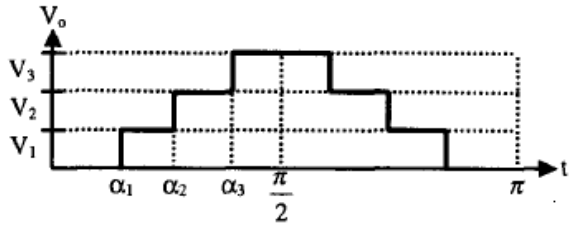


Figure 2. Positive half cycle of a seven level stepped output of multilevel inverter

Fourier series is used to find the odd harmonics using the waveform shown in figure 2. [2]

$$hn = \frac{4}{n\pi}[V1\cos(n\alpha 1) + V2\cos(n\alpha 2) + V3\cos(n\alpha 3)] \quad (1)$$

where n is the order of odd harmonics and α1, α2, α3 are the switching angles. V1, V2 and V3 are the voltage at different levels. α1<α2< α3<π/2

Modulation index can be found out by the equation

$$M = \frac{h1}{mVdc} \quad (2)$$

Where M is the modulation index, h1 is the fundamental component, m is the number of switching angle and Vdc is the DC voltage source used.

For removing the fifth and seventh odd harmonics these equations are written for fifth and seventh order and is equated to zero as shown in (3) to (5)

$$\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3) = \frac{3(1)\pi}{4} \quad (3)$$

$$\cos(5\alpha 1) + \cos(5\alpha 2) + \cos(5\alpha 3) = 0 \quad (4)$$

$$\cos(7\alpha 1) + \cos(7\alpha 2) + \cos(7\alpha 3) = 0 \quad (5)$$

When these equations are solved using newton Raphson computational method the value of α1, α2, α3 are obtained as 11.68˚, 31.18˚ and 58.58˚. [2],[7].

III. SIMULATION AND RESULTS

A. Cascaded topology with and without selective harmonic reduction

The simulink model of cascaded multilevel topology is shown in figure 3 and the pulse generator used in the simulink produces the pulse which is as shown in figure 4

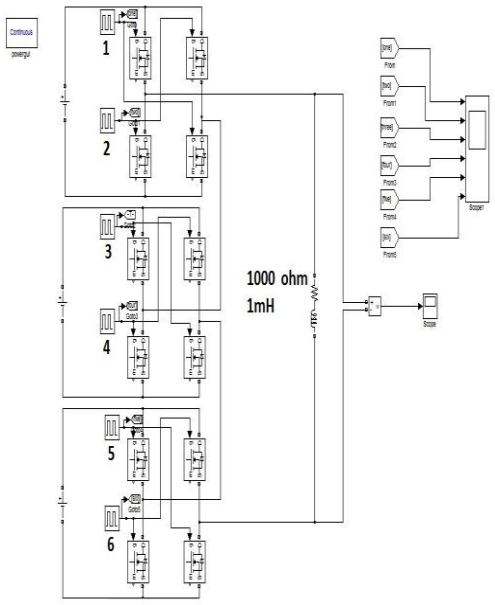


Figure 3. Simulink model of cascaded multilevel topology

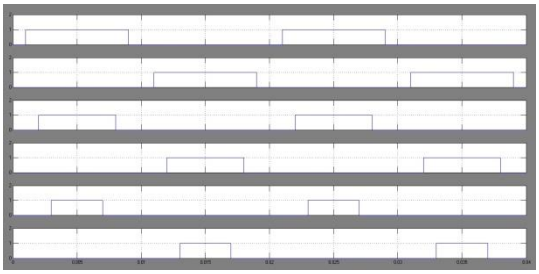
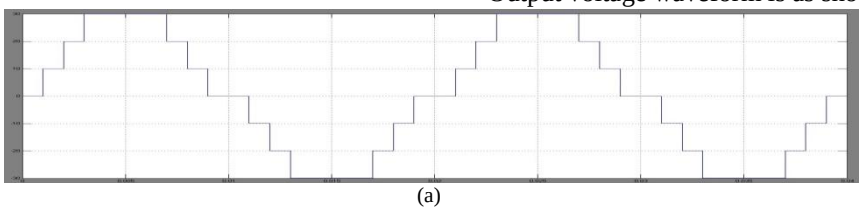
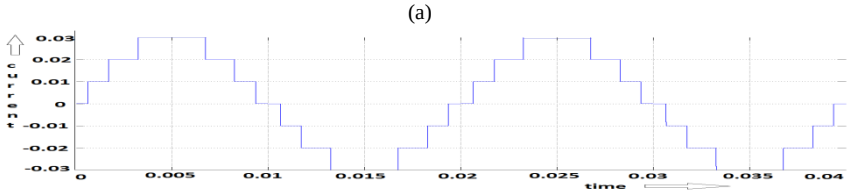


Figure 4. Pulse generated using pulse generator

Output voltage waveform is as shown in figure 5



(a)



(b)

Figure 5(a) Voltage waveform (b) Current waveform

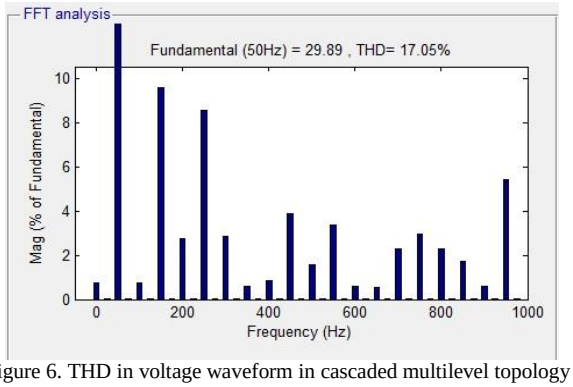


Figure 6. THD in voltage waveform in cascaded multilevel topology

Cascaded topology incorporating selective harmonic reduction can be implemented in the above simulink model by replacing pulse generators by a MATLAB function block. The switching angles found for modulation index=1 is 11.68˚, 31.18˚ and 58.58˚. These angles are used in MATLAB function block so as to switch the switches in such a way that one switch switches only once in a cycle [2].

THD of the voltage waveform when incorporating selective harmonics reduction is as shown in figure 7. When observing the voltage waveform of cascaded multilevel topology with and without selective harmonic reduction, waveform appears to be same but THD has been reduced to 14.02% in case of topology with selective harmonic reduction. This may be because of reducing the number of times the main switches switch in a cycle.

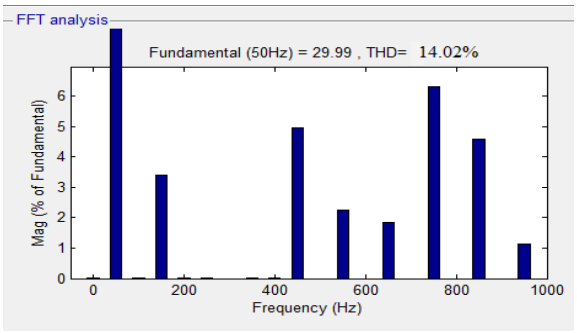


Figure 7. THD of voltage waveform for cascaded multilevel inverter incorporating selective harmonic reduction

B. Multilevel inverter using series connected sub-multilevel topology with and without selective harmonic reduction

Simulink model of multilevel inverter using series sub-multilevel topology incorporating selective harmonic reduction is as shown in figure 8. Load used here is 1000ohm and 1mH in series.

The voltage and current waveform of multilevel inverter using series sub-multilevel topology incorporating selective harmonic reduction is as shown in figure 9. The switching sequence is as shown in the table I

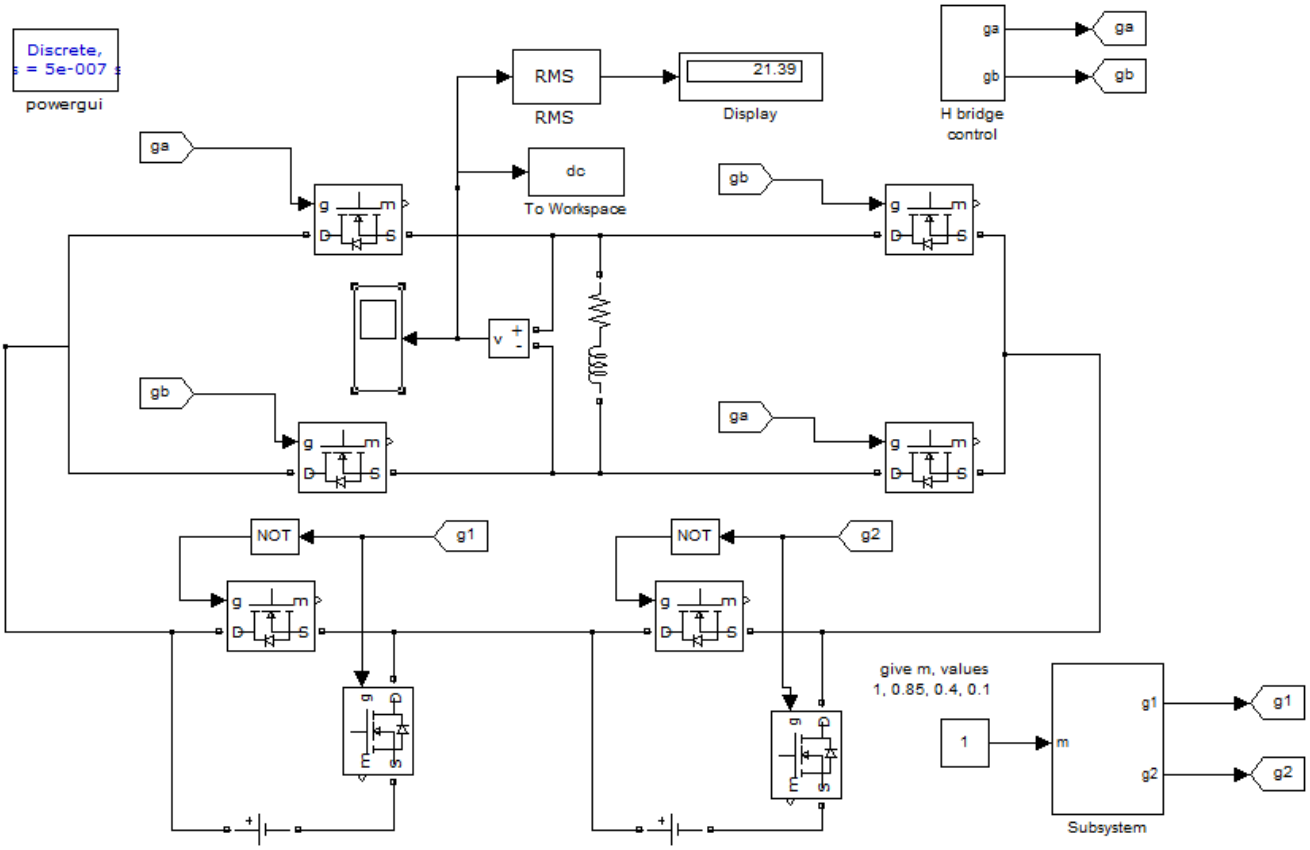
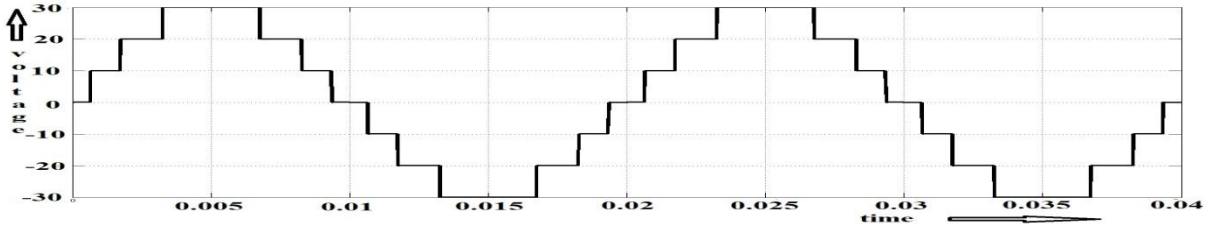


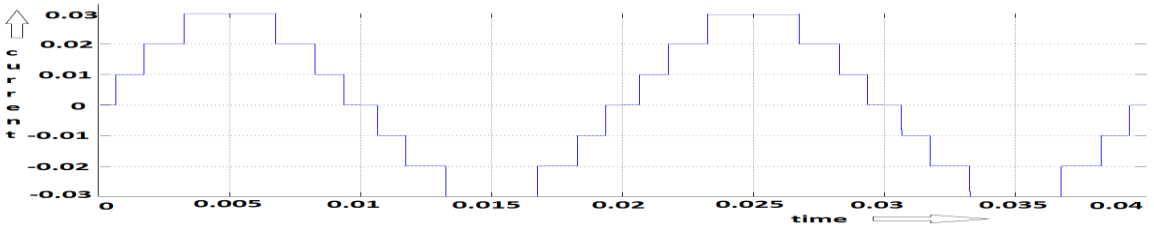
Figure 8. Simulink model of multilevel inverter using series sub-multilevel topology with selective harmonic reduction

TABLE I. VOLTAGE LEVEL FOR STATE OF SWITCHES

Voltage level	G1	G2	G1'	G2'	Ga	Gb
0	0	0	1	1	1	0
10	1	0	0	1	1	0
20	0	1	1	0	1	0
30	1	1	0	0	1	0



(a)



(b)

Figure 9 (a) voltage waveform (b) current waveform multilevel inverter using series sub-multilevel topology incorporating selective harmonic reduction

THD of the voltage waveform for multilevel inverter using series sub-multilevel topology incorporating selective harmonic reduction is as shown in figure 10

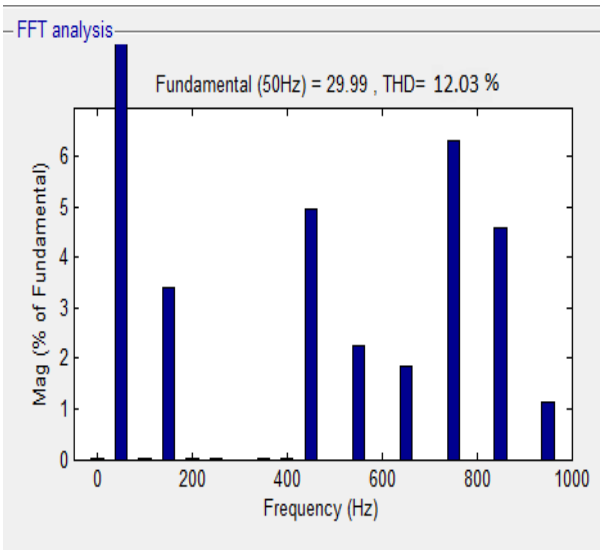


Figure 10. THD of the voltage waveform for multilevel inverter using series sub-multilevel topology incorporating selective harmonic reduction

Multilevel inverter using series sub-multilevel topology without selective harmonic reduction can be done using the figure 8 simulink model where the MATLAB function block is replaced by the pulse generator and providing pulses to the switches [1].

THD of the voltage waveform for multilevel inverter using series sub-multilevel topology without selective harmonic reduction is as shown in the figure 11

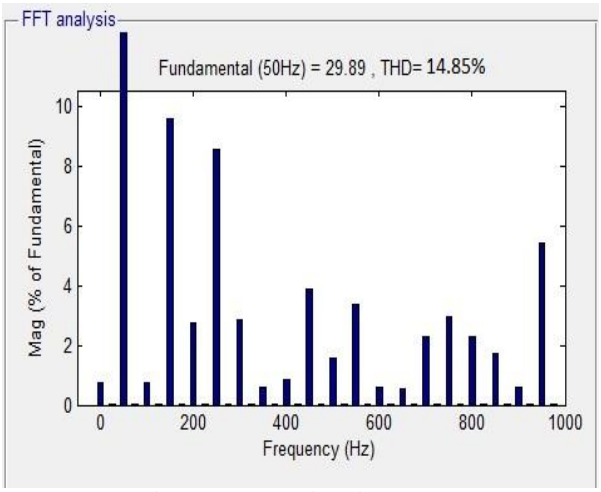


Figure 11.THD of the voltage waveform for multilevel inverter using series sub-multilevel topology without selective harmonic reduction

Even though the voltage and current waveform appears to be same for multilevel inverter using series sub-multilevel topology with and without using selective harmonic reduction, THD has been reduced to 12.03% in case of topology with selective harmonic reduction. This may be because of reducing the number of times the main switches switch in a cycle.

THD is reduced in case of multilevel inverter using series sub-multilevel topology when compared to cascaded topology as the number of switches required to produce seven level is reduced in case of series sub-multilevel topology when compared to cascaded topology. As the number of switches gets reduced switching losses decreases, harmonics reduce, control complexity decreases.

Comparison is done between sub-multilevel topology and cascaded topology with and without selective harmonic reduction at modulation index=1 and it is tabulated as below.

TABLE II COMPARISON BETWEEN SUB-MULTILEVEL TOPOLOGY AND CASCADED TOPOLOGY WITH AND WITHOUT SELECTIVE HARMONIC REDUCTION AT MODULATION INDEX=1

	Cascaded multilevel inverter without selective harmonic reduction	**Cascaded multilevel inverter with selective harmonic reduction**	**Sub-multilevel topology without selective harmonic reduction**	**Sub-multilevel topology with selective harmonic reduction**
Number of switches	12	12	8	8
Switching losses	High	Low	Low	Very low
THD	17.05	14.02	14.85	12.03
Voltage waveform	Same	Same	Same	Same
Current waveform	Same	Same	Same	Same
Control complexity	High	High	Low	Low
Efficiency	Very Low	High	High	Very high
Filter size	Very Large	Small	Small	Very small
Odd harmonic removed	Nil	5^{th} and 7^{th}	Nil	5^{th} and 7th

IV. CONCLUSION

This paper presents the comparison of multilevel inverter in cascaded and series sub-multilevel topology with and without selective harmonic reduction. Series sub-multilevel topology is good when compared to cascaded topology as the number of switches is less. Topology incorporating selective harmonic reduction is good when compared to topology without selective harmonic reduction as odd harmonics causing the considerable harmonics can be eliminated and switches switch only once in a cycle which again reduces the harmonics. It was found that the multilevel inverter with series sub-multilevel topology with selective harmonic reduction is having the minimum THD and hence this combination would be the best for all applications where multilevel inverter is to be used

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